

Enhancing MPI Communication using Accelerated Verbs: The MVAPICH Approach

Talk at UCX BoF (SC '18)

by

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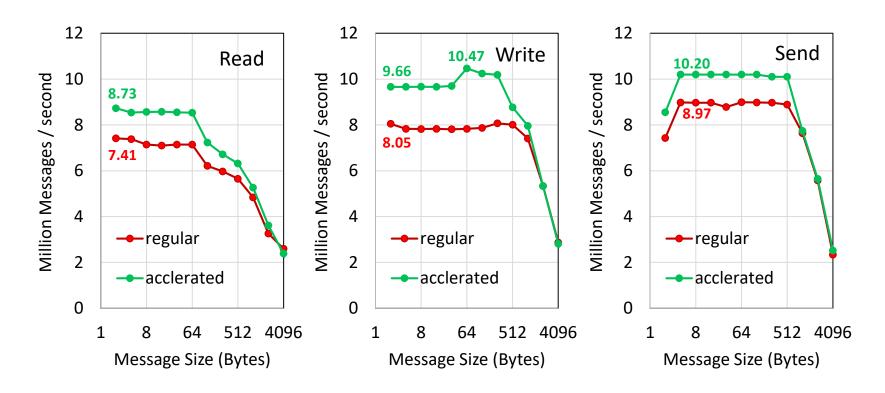
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Introduction, Motivation, and Challenge

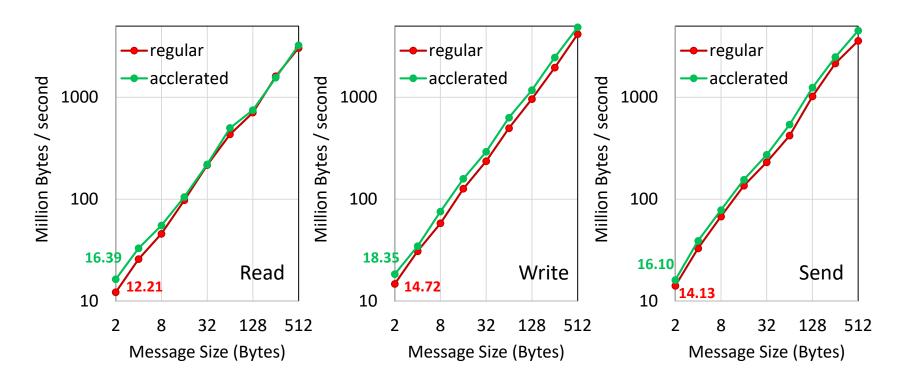
- HPC applications require high-performance, low overhead data paths that provide
 - Low latency
 - High bandwidth
 - High message rate
- Hardware Offloaded Tag Matching
- Different families of accelerated verbs available
 - Burst family
 - Accumulates packets to be sent into bursts of single SGE packets
 - Poll family
 - Optimizes send completion counts
 - Receive completions for which only the length is of interest
 - Completions that contain the payload in the CQE
- Can we integrate accelerated verbs into existing HPC middleware to extract peak performance and overlap?

Verbs-level Performance: Message Rate



ConnectX-5 EDR (100 Gbps), Intel Broadwell E5-2680 @ 2.4 GHz MOFED 4.2-1, RHEL-7 3.10.0-693.17.1.el7.x86_64

Verbs-level Performance: Bandwidth



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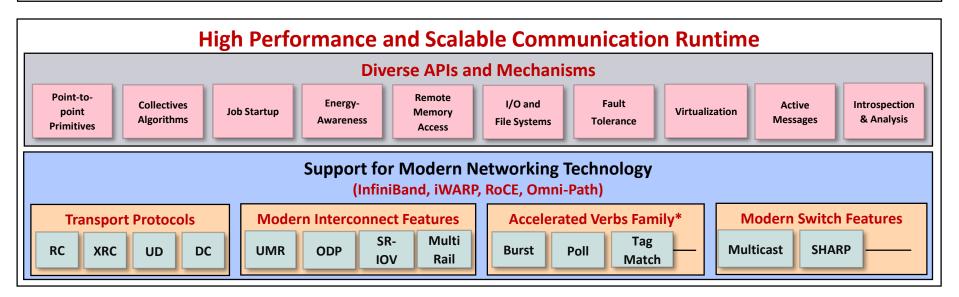
The MVAPICH Approach

High Performance Parallel Programming Models

Message Passing Interface
(MPI)

PGAS
(UPC, OpenSHMEM, CAF, UPC++)

Hybrid --- MPI + X
(MPI + PGAS + OpenMP/Cilk)



^{*} Upcoming